New Low Noise FET Structure

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ABSTRACT

A new monolithic FET topology has demonstrated a better minimum noise figure than a conventional Pi-gate FET. The new structure, named a Spider FET because of its gate feed configuration, has allowed an improved noise figure using the current 0.5 micron ion-implant production process.

DESCRIPTION

The spider FET, shown in Figure 1, consists of ten gate fingers, 30 microns long, arrayed in two rows of five with two vias providing ground. The structure is very compact allowing large devices to be fabricated in a small area. The gate feed structure incorporates the gate pad to minimize parasitics. The sources are connected through the vias; this allows the in-process DC probe measurements, completed prior to via formation, to be performed on a smaller device. Thus, the oscillations associated with large devices are eliminated. The drains are connected by an airbridge, since large devices have had oscillations when the drains were left unconnected at one end. The oscillations occurred when the drain line reached a quarter wavelength. Oscillations in excess of 60 GHz have been observed. All observed oscillations have been eliminated by strapping the drain line at both ends on devices up to 1200 μm.

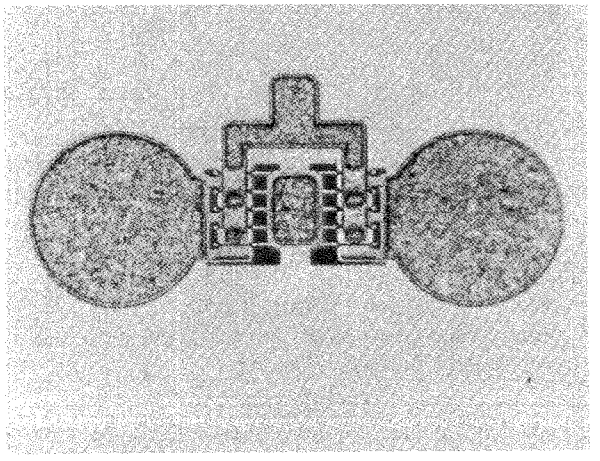

Figure 1. 300 μ Spider FET

The spider FETs are processed on ion-implanted low-noise profile material with Texas Instruments (TI) standard low-current gate recess on 6-mil GaAs. The gate length is 0.5 micron with a gate width of 300 microns. The source-drain spacing is 3 microns with the gate offset toward the source by 0.5 micron to reduce the source resistance. Boron isolation was used to define the active regions. The total device size is 0.012 by 0.025 inches (0.3 X 0.63 millimeters).

THEORY

The minimum device noise figure, F_{min}, is dominated by the transconductance (g_m), the gate-to-source capacitance (C_{gs}), and the parasitic gate and source resistances (R_g and R_s). From Fukui [1]:

$$F_{min} = 1 + k_1 f C_{gs} \sqrt{(R_g + R_s)/ g_m}$$

$$R_n = k_2 / g_m$$

$$R_{op} = k_3\left(\frac{1}{4g_m} + R_g + R_s\right)$$

$$X_{op} = \frac{k_4}{f C_{gs}}$$

where k_1, k_2, k_3, and k_4 are fitting factors.

In low noise FETs reduction of the source resistance R_s is accomplished by offsetting the gate toward the source in the channel and by providing low resistance ohmic contacts for the source. As mentioned previously, the spider FETs gate is offset 0.5 μm toward the source. The values of g_m and C_{gs} in a FET are dominated by the gate length and doping profile. Parasitic capacitance from the gate feeds and gate pad area, although a secondary contributor to C_{gs}, are still important and the spider FET layout minimizes this term. The gate pad is of minimal size and all gate feeds contact the gate pad directly without any additional routing. Compare the Pi-type 300 μm X 0.5 μm FET in Figure 2 where significant routing of the gate feeds is required. The spider FET topology reduces the gate resistance over a Pi-FET by providing a plated gate feed

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and a large number of gate fingers. The spider FET also allows a more compact FET requiring much less space than a similar Pi-FET, especially in 600 and 1200 micron versions with only two vias required. Concurrent with these advantages is an increase in the output capacitance C_{ds}. Because C_{ds} directly affects device gain but has very little impact on noise figure, a trade off was made to optimize device noise figure.

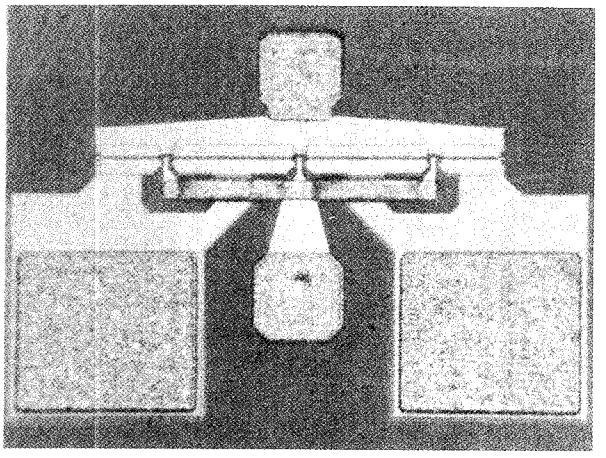

Figure 2. 300 μ Pi Gate FET

RESULTS

The spider FET is compared to a standard process 0.5 micron pi-gate FET and a commercial 0.35 micron pi-gate HEMT in Figure 2. F_{min} and maximum gain at F_{min} for the three FET types are shown in Figure 3. The spider FET has a noise figure that is higher than the 0.35 micron HEMT but significantly better than the 0.5 micron pi-gate FET. The associated gain at minimum noise figure is less for the spider FET when compared to the 0.5 micron pi-gate FET. However, it should be noted that the spider FET can be matched for a greater gain than the 0.5 micron pi-gate FET and still have a better noise figure. A model of the spider FET has been generated and is compared with the 0.5 micron pi-gate FET and the 0.35 micron pi-gate HEMT in Table 1. Figure 4 shows the lumped element model. The optimal bias for minimum noise figure operation of each device is included in Table 1 and the models are for these bias conditions. This data and model were developed using measured data on nine devices from three slices for the spider FET; five 0.35 micron HEMT devices were obtained commercially, and large numbers of 0.5 micron pi-gate FETs were obtained from numerous slices.

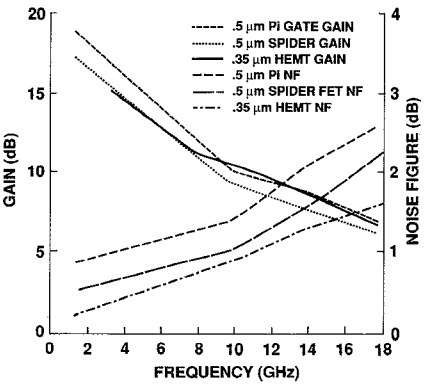

Figure 3. Comparison of Spider FET eith .35 + .5 mm P + FETs

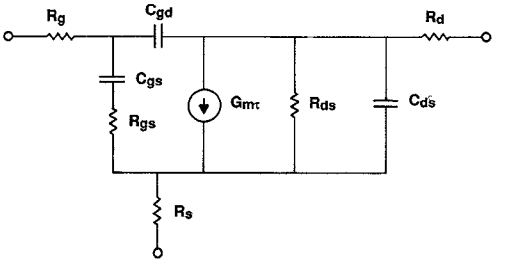

Figure 4. Lumped Element Model

TABLE 1. LOW NOISE FET MODEL COMPARISON

ELEMENT	MITSUBISHI 0.35 μm HEMT 3V, 15 mA	EG-1350 3V, 10 mA	SPIDER FET 3V, 10 mA
Cgs	0.26	0.35	0.35
Cgd	.027	.025	.044
Cds	.089	.075	0.09
gm	0.73	.047	.054
Rgs	1.0	4.0	0.5
Rds	210	230	256
Rg	3.0	1.5	0.6
Rs	2.8	3.1	2.9
Rd	2.9	4.0	4.4
DC PARAMETERS			
Idss	40 mA	54 mA	53 mA
Vpo	1.1 V	1.4 V	1.4 V

CONCLUSION

A new topology for the FET has been presented that has demonstrated better minimum noise figure than the conventional pi-gate low-noise FET. This topology can be incorporated into monolithic circuits and allows easy implementation of feedback and self bias networks. The Spider FET topology is ideally suited for the upcoming 0.25 μm gate processes and HEMT technology to achieve improved minimum noise figures.

REFERENCES

[1] H. Fukui, "Design of Microwave GaAs MESFETs for Broad-Band Low Noise Amplifiers," IEEE Trans. MTT-27, July 1979, pp.643-650.